

Competitiveness centers, a way to reach SMBs

INRIA is making more global investments in the competitiveness centers in an effort to enhance its technology transfer activities with SMBs. The Minalogic center in Grenoble is a good example of this. It is based on the unusual combination of micro-nanotechnology with embedded intelligent systems software.

The goal of the Minalogic world competitiveness center is to shift the competitive battlefield from that of production costs to speed of innovation, and to become the top European center, as well as one of the world's most prominent, for intelligent systems micro chips. It possesses strong advantages in doing so, since it rubs shoulders with a cutting-edge research environment and since leading industries in that field, such as HP, Bull and STMicroelectronics, are present in Grenoble. "Minalogic comprises 23 major corporations, 74 SMBs and 13 research and training centers, not to overlook the local institutions, R&D firms and venture capitalists who are also members of the center," adds Philippe Broun, manager for partnerships and innovative projects at INRIA's Grenoble center. "Fifteen teams from the Institute are participating in Minalogic's projects, and one of them, in which INRIA and one of its recent start-ups (Mil-Pix) are partners with an SMB in Grenoble, will soon receive a label." The Grenoble research center teams are participating in research on the "software and chip-embedded intelligent systems" aspects such as the Multival project for multi-processor platforms (cf. box on "Validating multi-processor architectures") and the Iglance project on 3D television that also involves the INRIA start-up 4DViews. As another example, Institute teams are participating in the Aravis

project on architectures for embedded high-performance computing systems. This project was awarded the center's green label, given to projects that serve to reduce or control energy usage. The Institute is also becoming more and more involved in projects related to the cluster's micro and nano technologies. A superb example of this is the Minimage project, focused on microelectronics and optics, which will help create an international outlet for the micro camera in Europe by means of leaders of industry, SMBs and public laboratories (cf. box "Tomorrow's micro cameras").

Run by their corporate sponsors and integrating a number of innovative SMBs, the competitiveness centers are, for the Institute, a key component of its strategy for technology transfer to SMBs (cf. article, Page 1). "They bring up the key innovation problems for a given industrial process and enable us to maintain contact with the SMBs that we are not very familiar with and for which we should be able to identify their needs in order to set up favorable conditions for transfers," explains David Monteau, manager for competitiveness center relations in the Department of Technology Transfer and Innovation. Participation in the centers allows INRIA to benefit from, and contribute to, a defining collective effort in developing innovations.

At Minalogic, the new national sector representatives hired by INRIA are already taking steps to identify innovative SMBs and put them in contact with INRIA research teams. "These people are working, for example, with the team at the Minalogic center, especially its SMB manager, in coordination with the industrial relations department at INRIA Grenoble," notes David Monteau. This work should be facilitated by the fact that Minalogic, just as INRIA, has made a commitment, through an SMB agreement, to promote innovation in SMBs. ●●●

VALIDATING MULTI-PROCESSOR ARCHITECTURES

Started on December 1, 2006, Multival is one of the first projects

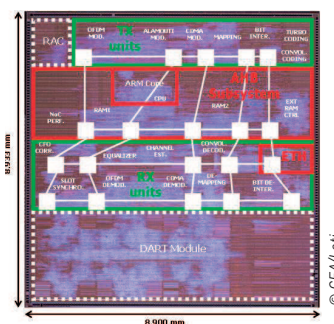
set up at the Minalogic center. Administered by STMicroelectronics, it also includes Bull and the CEA's LETI in working on CADP software developed by the Vasy team at INRIA. CADP (Construction and Analysis of Distributed Processes) provides verification tools for asynchronous systems (cf. Inédit, No. 58 and No. 60). The goal of this project is to use CADP to validate new multi-processor and multicore architectures. Bull is using it to design its Fame2 architecture destined, among other things, for use in the Tera 100 petaflop supercomputer. The CEA's LETI is using CADP to validate and co-simulate its chip-based network architectures, Faust and Magali. Lastly, STMicroelectronics is using it to verify and predict the performances of its multicore architecture, xSTream.

Multival has already contributed to considerably improving and

expanding CADP. "We have benefited from access to substantial human resources and very close collaboration with industry,"

emphasizes Hubert Garavel, manager of the Vasy team. "Following the engineers from Bull, it is now the turn of those from STMicroelectronics working on Multival to be guests at INRIA's Grenoble center. We thus collaborate on a daily basis. Our industry partners are heavily involved and want to include CADP in the development of their architectures." This goal would seem to be coming to fruition through the setting up by STMicroelectronics of regular seminars on this technology and of license

transfer agreements. Half-way there and it's already a great success!



→ CONTACT

Hubert Garavel, Vasy project-team, INRIA Grenoble—Rhône-Alpes
Tel.: + 4 76 61 52 24, Hubert.Garavel@inria.fr